ABSTRACT

0031 A contact interconnect structure including the method of providing a semiconductor substrate including CMOS devices including active contact regions; forming a first set of dielectric layers to form a first thickness for etching a first set of openings through a thickness thereof including a bottom portion having a maximum width of less than about 70 nanometers; etching the first set of openings to contact active contact regions; filling the first set of openings with a first metal; forming a second set of dielectric layers to form a second thickness for etching a second set of openings through the second thickness comprising a bottom portion having a maximum width of less than about 70 nanometers; etching the second set of openings to provide electrical communication with the first set of openings; and, filling the second set of openings with a second metal to form contact interconnects.